REMARKS

The Office Action of January 22, 2010 has been carefully considered by Applicants. Applicants may desire an opportunity to conduct one or more Examiner interviews to further prosecution of this case. Claims 1-9 and 11-30 have been rejected. Claims 1, 11, 13, 19, 20, 24, 26, 28, and 30 are amended. Claims 23, 25, 27, and 29 are canceled. No new matter has been added.

Claim Rejection under 35 U.S.C. § 112

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. Applicants have amended claim 1 to overcome this rejection. Accordingly, Applicants respectfully request that the Section 112 rejection be withdrawn.

Claim Rejection under 35 U.S.C. § 103(a)

Claims 1-9 and 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alcorn (U.S. Patent No. 6,149,522).

Applicants believe the rejection is deficient for the following reasons.

Applicants respectfully submit that a prima facie case of obviousness is not made. A reason as to why the recitation of "determining whether to hold said volatile programmable electronic device in a reset mode" would have been obvious over the cited art is not stated in the Office Action. The following is stated on pages 7 and 8 of the Office Action:

> Regarding the amendment, "determining whether to hold said volatile programmable electronic device in a reset mode," while Applicant's Specification, Page 29, Paragraph 56, discloses that the FPGA can be held in reset mode, the Specification goes on to disclose that in other embodiments, "holding of the FPGA in reset mode is presumable not possible, while in other embodiments, such a hold may be optional, or designed as mandatory, as desired." This is viewed as admission that placing the volatile device in reset mode is merely a design consideration.

> Therefore, since Applicant has disclosed that holding the volatile device in reset mode is optional, Examiner cannot but conclude that this have been a matter of obvious design choice to a person of ordinary skill in the art at the time of Applicant's invention.

Thus, it is initially indicated in the Office Action that holding an FPGA in a reset mode is a design consideration (see the conclusion of the Office Action's first paragraph quoted above). It is then stated in the Office Action that "since Applicants have disclosed that holding the volatile device in reset mode is optional, Examiner cannot but conclude that this have been a matter of ***obvious*** design choice" (Emphasis added). Applicants disagree. The feature is one of the different embodiments. Applicants respectfully disagree with the Examiner's characterization, and submit that the Examiner has not presented that the feature is obvious in the context of all elements of the claim.

Applicants respectfully submit that no reason is provided as to why the feature of "determining whether to hold said volatile programmable electronic device in a reset mode" is obvious. This feature is supported on page 9, paragraph 56 of the specification. Hence, Applicants respectfully submit that a prima facie case of obviousness is not made and respectfully request that the Examiner provide a reason as to why the feature of "determining whether to hold said volatile programmable electronic device in a reset mode" would be obvious.

The Examiner further states on page 10 of the Office Action:

> **Claims 23-30:** These claims require determining when the FPGA is placed in reset mode & when it is removed from the reset mode. As explained above with respect to claim 1, however, since Applicant disclosed that holding the FPGA in reset mode is optional, (See Specification, Page 29, Paragraph 56), these limitations would have been matters of obvious design choice to a person of ordinary skill in the art at the time of Applicant's invention.

Again, no reason is provided as to why claims 23-30 would have been obvious over the cited art. Rather, the specification is cited to determine that claims 23-30 would have been obvious. Applicants own specification cannot be used to establish a prima case of obviousness because the Applicants specification is not prior art. Thus, Applicants respectfully submit that a prima facie case of obviousness is not made with respect to claims 23-30.

Moreover, claims as amended describe limitations, such as recited in claim 1, "continuing to hold said volatile programmable electronic device in the reset mode until said confirming of said successful comparison is completed". Applicants believe the citations providing by the Examiner don't teach or suggest a microprocessor based machine, such as a gaming machine, in the manner as described in the pending claims.

As described in the claims, a volatile programmable electronic device, such as a field programmable gate array, is disposed in a communication path between a CPU and a memory device storing the executable programming instructions for generating the wager-based game (see FIG. 3 of the pending application). The volatile programmable electronic device comprises a plurality of logic elements to form logic gates. The volatile programmable electronic device may be programmed to enable communications between the CPU and the memory device storing executable programming instructions for generating the wager-based game. Further, the operating contents of the volatile programmable electronic device may be held as substantially empty upon a shut down phase of the gaming machine to disable communication between the central processing unit and the memory device. In addition, the volatile programmable electronic device is configured to monitor communication between the central processing unit and at least one of an input device and an output device. Further, there is a comparison of at least a representative portion of data from a configuration file with at least a representative portion of data from a custodial file. There is also a confirmation of whether the configuration file has been successfully compared to the custodial file. The volatile programmable electronic device is continuously held in the reset mode until the confirmation of the successful comparison is completed. Applicants believe that the prior art citations provided by the Examiner do not teach or suggest a gaming machine configured with a volatile programmable memory device that is used in this manner.

CONCLUSION

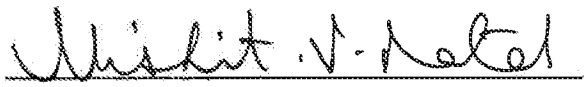
Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

The Commissioner is hereby authorized to charge any additional fees, including any extension fees, which may be required or credit any overpayment directly to the account of the undersigned, No. 504480 (Order No. IGT1P096/P000824-001).

Respectfully submitted,
Weaver Austin Villeneuve & Sampson LLP
/Reginald J. Suyat/

Reginald J. Suyat
Registration No. 28,172

Respectfully submitted,



Nishitkumar V. Patel
Reg. No. 65,546
P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100